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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02078657.0

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Method of operating a driving circuit for a display system, driving a circuit in which this method is applied and apparatus comprising such a driving circuit

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Method of operating a driving circuit for a display system, driving circuit in which this method is applied and apparatus comprising such a driving circuit

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The invention relates to a method of operating a driving circuit for a display system, wherein a sequence of writing and/or reading video data in, respectively out of a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line.

This method is applied in display systems such as Cathode Ray Tubes (CRT), Plasma Discharge Panels (PDP), Liquid Crystal Displays (LCD), one-panel Liquid Crystal on Silicon (LCOS). All of them require different addressing sequences. As driving circuits for these display systems frame memories are wildly used. As frame memory often external or embedded static or dynamic random access memories (SRAM's or DRAM's) are used for re-ordering video information. Sequencers normally control the order of reading and writing. When the driving circuit is supposed to work with different resolutions, e.g. zooming or split screen monitoring, or it must be able to drive different kinds of the above mentioned displays, a flexible addressing of the frame memory is needed for re-ordering pixel data. Particularly the driving circuit must be flexible enough to generate sequences such as interlaced sequences and color sequential sequences, and flexible enough to handle design changes, for example, in the optical lay out of the LCOS system.

A possible solution may be found in the design of the sequencer by a number of counters combined with logic. However, the difficulty thereof is that this is basically a non-flexible solution. The different sequences to be produced have to be known in advance to guarantee a coverage of all required solutions.

Another possible solution may be a sequence table approach, wherein the whole sequence is stored into a random access memory that is part of the sequencer. This solution offers in principle all the required flexibility. Such a solution is known from US patent 5,587,962. This patent specification discloses a device with a frame memory circuit which permits limited random access and that is used to perform a wide variety of special effects video applications. The frame memory circuit of this device stores and provides

streams of data and supports both serial access and random access. A data input of a random access memory array couples to a data buffer so that the data buffer may synchronize operation of the memory array with the streams of data. An address input of the random access memory array couples to one address sequencer which generates a sequence of memory addresses that are successively applied to the memory array. An address buffer register also couples to the address sequencer. US patent 5,587,962 provides a memory circuit which serves as a frame memory and permits special effects like zoom or split screen and other to be performed efficiently. For that, the memory circuit represents a single chip integrated circuit that contains 2^{20} bits of memory storage organized as 262,144 four bit wide words with special write and read access arrangements. The memory circuit generally operates in a serial access mode for both write and read operations but has particular features which permit random access for writing or reading of the memory circuit on a limited scale. For receiving analog video signals converted to digital pixels, the memory circuit includes a serial pixel data input, which supplies four bits of data per pixel. Serial pixel data input couples to an input port of a write serial latch, and an output port of write serial latch couples to an input port of a write register. An output port of the write register couples to a data input port of a memory array. The memory array is dynamic random access memory array containing 2^{18} four bit memory locations. A data output port of the memory array couples to a data input port of a read register, and a data output port of a read register couples to a data input port of a read serial latch. The arbitration and control circuit passes an address generated by the address generator to the memory array so that the data may be written into the memory array, but a delay may occur due to refresh operations or read accesses of the memory array. Accordingly, arbitration and control circuit may additionally contain storage devices so that addresses generated by address generators are not lost when immediate access to the memory array is blocked. US patent 5,587,962 discloses a table based solution. The solution is table based because the whole sequence is stored on a DRAM memory array that is part of the frame memory circuit. As described above the solution offers in principle all the required flexibility. However, this solution has the disadvantage that the size of the table must be relatively large. For example, an UXGA-based LCOS design has 1200 lines, so the table has to have 1200 entries of, in practice, 21 bit each, resulting in a table of about 25 kbit.

The purpose of the invention is provide for a method of operating a driving circuit with a sequencer as described in the opening paragraph, which has the flexibility of the above table-based sequencer, but is less expensive.

Therefore, according to the invention, this method is characterized in that by means of switching means the driving circuit is alternately operated in a first mode wherein in the address sequencer addresses for the video data in the memory are generated by combining line pointers out of block of line pointers in address table register means with the output of pixel counting means and in a second mode wherein a block of line pointers out of a full table of line pointers in said memory is downloaded into said address table register means.

As already mentioned, the invention further relates to a driving circuit for a display system, wherein the method according to the invention is applied. This driving circuit comprises a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, and is characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers out of said table of line pointers, means for successively updating the address table register means with next blocks of line pointers, and pixel counting means, the output of which in combination with the successive line pointers from the address table register means determines the addresses for said video data. Particularly, switching means are provided, by means of which alternately in a first mode in the address sequencer memory addresses for video data are generated and in a second mode the address table register is updated with a next block of line pointers. In a practical embodiment, the full table of line pointers for different sequences of video data to be displayed will be incorporated in the memory.

The invention also to an apparatus for displaying images comprising a display system and a driving circuit as described above.

The invention further relates to an algorithm for processing addresses in said driving circuit and said apparatus. He invention also relates to a computer program capable of running on signal processing means in said driving circuit, and to an information carrier, carrying said computer program.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment described hereinafter, wherein

Fig. 1 shows the system set up of a driving circuit for a display according to the invention in normal operation;

Fig. 2 shows the system set up of the driving circuit for address transfer;

Fig. 3 shows a flow diagram for the applied method during normal operation;

Fig. 4 shows a flow diagram for the applied method during reading of a table block from the main memory into the address table register;

Fig. 5 shows a flow diagram for the applied method illustrating the repeatedly executed address table block transfer;

Fig. 6 shows an apparatus provided with a driving circuit according to the invention.

Fig. 1 shows the system set up of a driving circuit for a display in normal operation comprising a main memory 1 and an address sequencer 2. The main memory 1 includes a frame memory 3. Video data is stored in the frame memory 3 is a first sequence and read out thereof in a second sequence. The frame memory addresses therefore are generated by the address sequencer 2. In the present embodiment the video data is formed by progressive video signals with one component, the luminance (Y) component, which signals for the sake of simplicity are supposed to be written sequentially and read out interlaced or color-sequential. Alternatively, an interlaced signal could be converted into a progressive signal by applying the present invention.

The address sequencer 2 is provided with an address table register 4 containing a table of line pointers. These line pointer form part of the frame memory addresses, indicating line addresses. During normal operation subsequent line pointers are read out of address table register 4 by means of a line counter 5 and supplied to a first entry of an adder 6. A pixel counter 7 is coupled with the second entry of the adder 6. The subsequent output signals of the adder 6 represent the frame memory addresses for the frame memory 3. The subsequent frame memory addresses determine the sequence in which video signals stored into the frame memory 3 are read out thereof or the sequence in which video signals supplied to the frame memory 3 are stored therein.

When, for example, the system is applied in combination with a display having 480 lines, the line counter 5 runs from 0 to 479; when one line contains 720 pixels, the pixel counter 7 runs from 0 to 719. When the address table register 4 would contain 480 line addresses of usually 21 bits, a table of about 10 kbit would be necessary, which is relatively expensive. With a display of 1200 lines and in case the address table register 4

would contain 1200 line addresses of 21 bits, a table of about 25 kbit would be necessary. According to the invention the number of line pointers in the address table register 4 is limited, for example to 32; this results into an address table of about 0,7 kbit. So, the address table register 4 can only contain blocks of line pointers. This, however, requires constantly an updating of the address table register 4; for reading out a frame of 480 lines the address table register 4 must be updated for 15 times. To make this possible all line pointers are stored in the main memory 1. Each time a block of line pointers is successively read out of address table register 4, a next block of line pointers is transferred from the main memory 1 into the address table register 4. This process, the system set up for (line) address transfer, will be clarified with reference to fig. 2. Both the system set up in normal operation and the system set up for address transfer occur under control of a control processor 8, being part of the address sequencer 2.

Fig. 2 shows the system set up for address transfer. When the last line pointer of a block of lines pointers in the address table register 4 is read out, the address sequencer 2 reads a new block of line pointers from the main memory 1, i.e. a next block of line pointers is downloaded into the address table register 4. This requires a base address register 9, containing the base address or start address for a block of line pointers in the main memory 1, and an address counter 10. By means of an adder 11 the addresses for the line pointers in the main memory 1 are formed and supplied thereto in the read mode (read = 1 in fig. 2) of the frame memory 3. These addresses represent an index for the line pointers in the frame memory 3. This index is as large as the number of lines of the display. In the write mode (read = 0), the addressed line pointers are transferred into the address table register 4. So, the whole system is constantly switching between the table update mode and the address sequence mode (the normal mode).

Fig. 3 shows the flow diagram for the applied method during normal operation. During initialization the line counter 5 is reset to i = 0. The next step is the generation of the successive frame memory or pixel addresses (k= 0 ... N-1, wherein N is the number of pixels of a line) for a first line and the video data transfer realized by means of these addresses. Thereafter the line counter 6 is increased by 1 (i:=i+1) and the frame memory or pixel addresses for the next line are generated, realizing a corresponding video data transfer. This process continues till the frame memory or pixel addresses for the last line are generated. When the last line is reached the loop has finished.

Fig. 4 shows the reading of a block of line pointers out of the main memory 1 into the address table register 4. During initialization the base address in base address register

9 for a block of line pointers is reset to j = 0. Then, during (line) address transfer, the line pointer corresponding to base address j = 0 is read from the frame memory 1 into the address table register 4. Thereafter, the base address is successively increased by 1 (j:=j+1) and the corresponding line pointers are read from the main memory 1 into address table register 4. This loop continues until the last line pointer of the block of line pointers is downloaded in address table register 4.

Fig. 5 shows the flow diagram for the applied method illustrating the repeatedly executed address table block transfer. During initialization the block of line pointers in address table register 4 is moved into the main memory 1 and the line counter 5 is reset to i = 0. Then the loop for video data transfer starts. First block 1 is read from the main memory 1 into address table register 4. Then video data corresponding with block 1 is transferred to the display. Thereafter, successively, next blocks of line pointers are downloaded and the video data corresponding with these blocks are transferred. After that the last block of line pointers id downloaded and the corresponding video data is transferred, the loop is finished.

Fig. 6 shows an apparatus 100 for displaying images including the driving circuit according to the invention. The apparatus 100 comprises a display 101, a main memory 1 with a frame memory 3 and an address sequencer 2. For example, the display 101 is chosen out of the group consisting of CRT, PDP, one-panel LCOS. The address sequencer 2 and the frame memory 3 are coupled for bi-directional data transfer, for example using a standard interface 102. The main memory 1 is also coupled with the display 101 for the transfer of video data.

The invention is not restricted to the preferred embodiment shown in the figures. Modifications are possible. As stated before, the address sequencer is composed of a picture line address part or line pointer and an address part for the pixels on a picture line. In the described embodiment the line pointer relates to a full address line and the pixel address part to all the pixels of a picture line. However, it may also be possible that the line pointer relates to part of a picture line, for example, half a picture line; in that case the pixel address part relates only to the pixels of half a picture line too. Also, the line pointer can relate to more than one, for example two picture lines; in that case the pixel address part relates to the pixels of two picture lines.

CLAIMS:

1. Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data in, respectively out of a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, characterized in that by means of switching means the driving circuit is alternately operated in a first mode wherein in the address sequencer addresses for the video data in the memory are generated by combining line pointers out of block of line pointers in address table register means with the output of pixel counting means and in a second mode wherein a block of line pointers out of a full table of line pointers in said memory is downloaded into said address table register means.

2. Driving circuit for a display system comprising a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers out of said table of line pointers, means for successively updating the address table register means with next blocks of line pointers, and pixel counting means, the output of which in combination with the successive line pointers from the address table register means determines the addresses for said video data.

3. Driving circuit as claimed in claim 2, characterized in that switching means are provided, by means of which alternately in a first mode in the address sequencer memory addresses for video data are generated and in a second mode the address table register is updated with a next block of line pointers.

4. Driving circuit as claimed in claim 2 or 3, characterized in that the memory comprise a full table of line pointers for different sequences of video data to be displayed.

5. Apparatus for displaying images comprising a display system and a driving circuit according to anyone of the claims 2-4.

6. Algorithm for processing addresses in a driving circuit for a display system according to anyone of the claims 2-4 and in the apparatus according to claim 5.

7. Computer program capable of running on signal processing means in a driving circuit for a display system according to anyone of the claims 2-4 or in the apparatus according to claim 5.

8. Information carrier carrying the computer program according to claim 7.

ABSTRACT:

A table based driving circuit for displays that switches between a normal operation mode and a read table block mode. The driving circuit comprises an address sequencer and a memory. The memory comprises the full table of different sequences, like interlacing of color sequential sequence. During the read table mode the next upcoming addresses are read, i.e. are downloaded, from the memory into an address table register in the address sequencer. During normal operation mode the address sequencer generates the addresses for the video data to be stored in the memory or to be displayed.

Fig. 1

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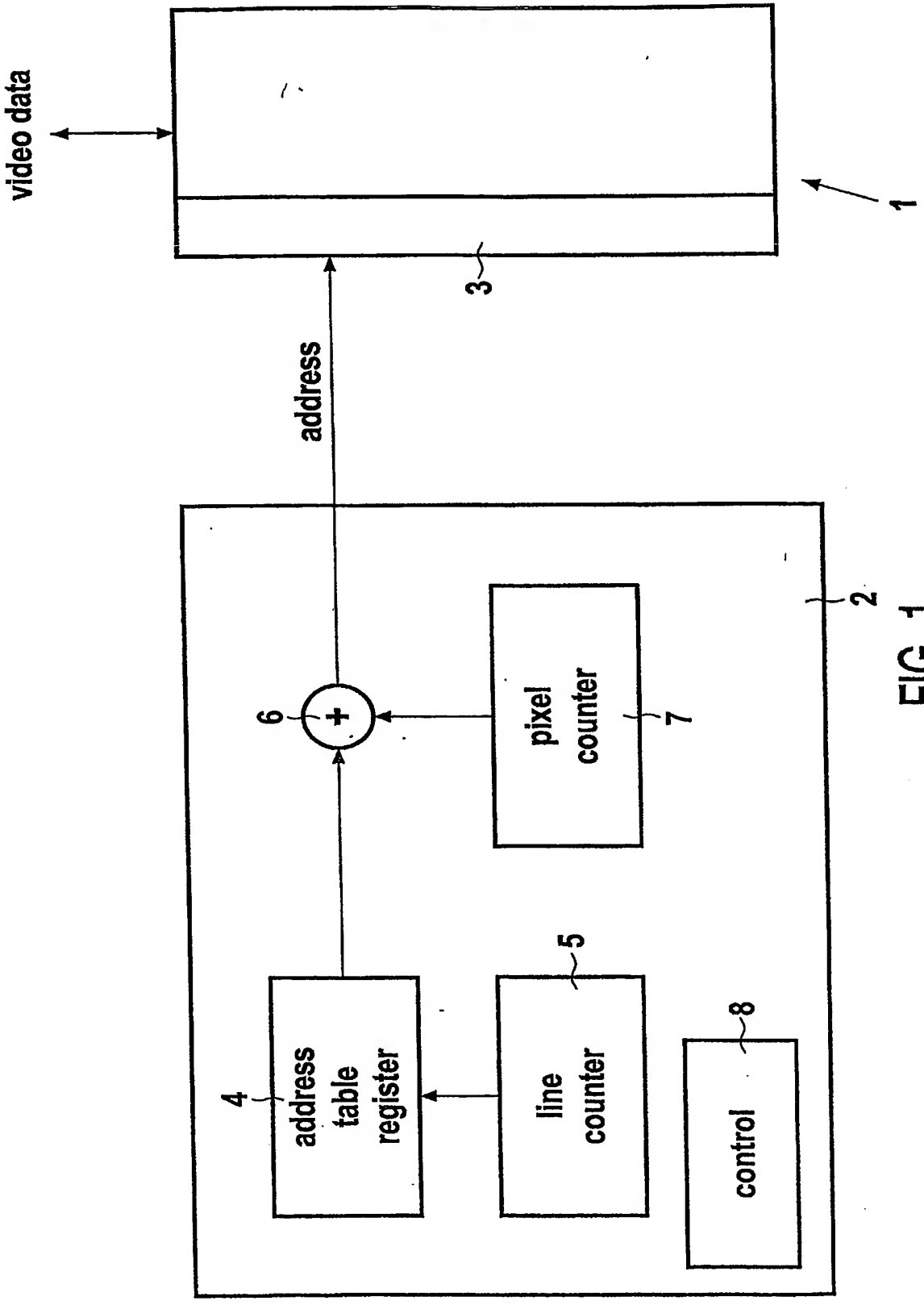

FIG. 1

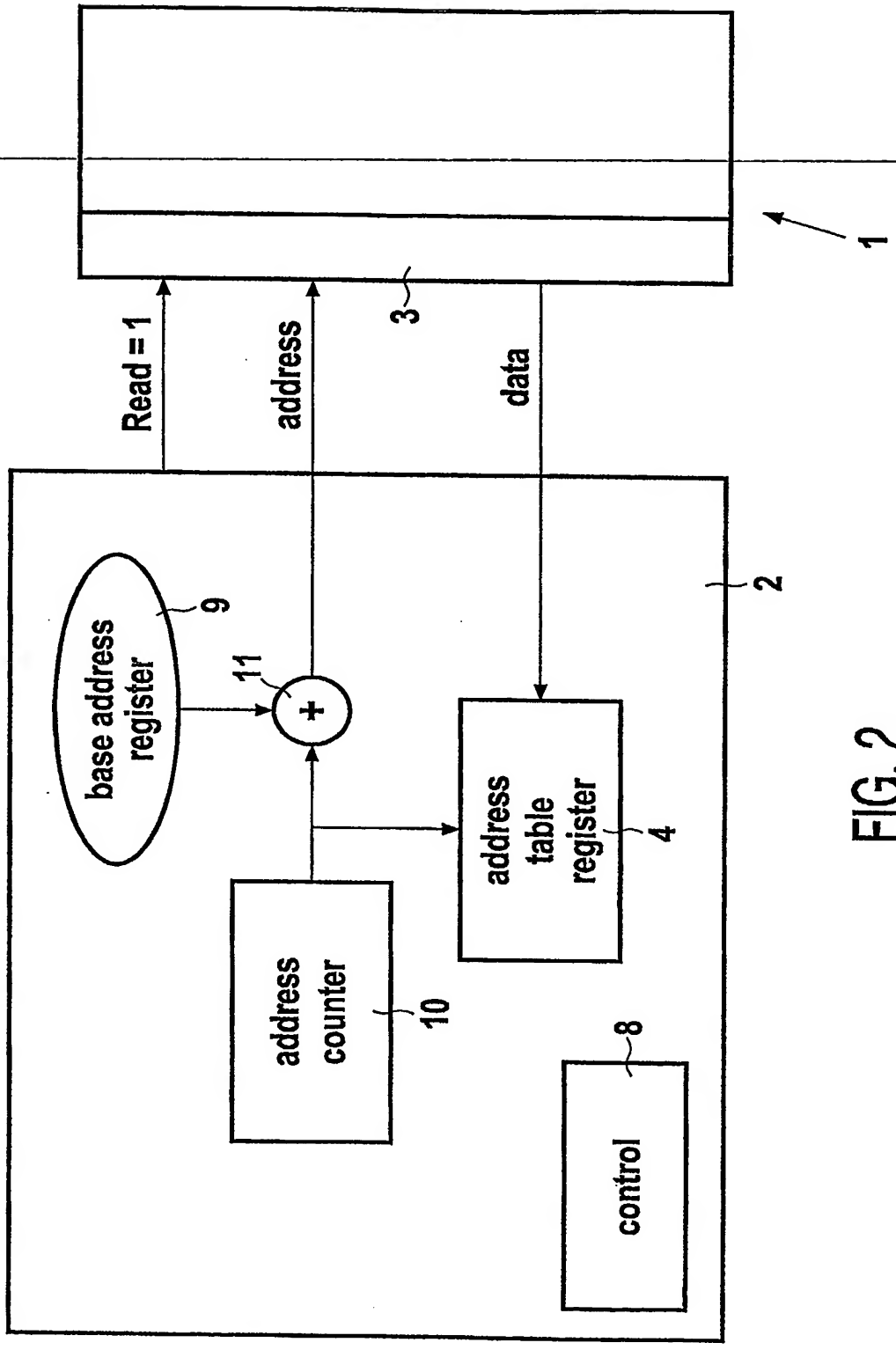
1
3
Read = 1
address
data
2
base address register
9
11
+
address table register
4
address counter
10
control
8

FIG. 2

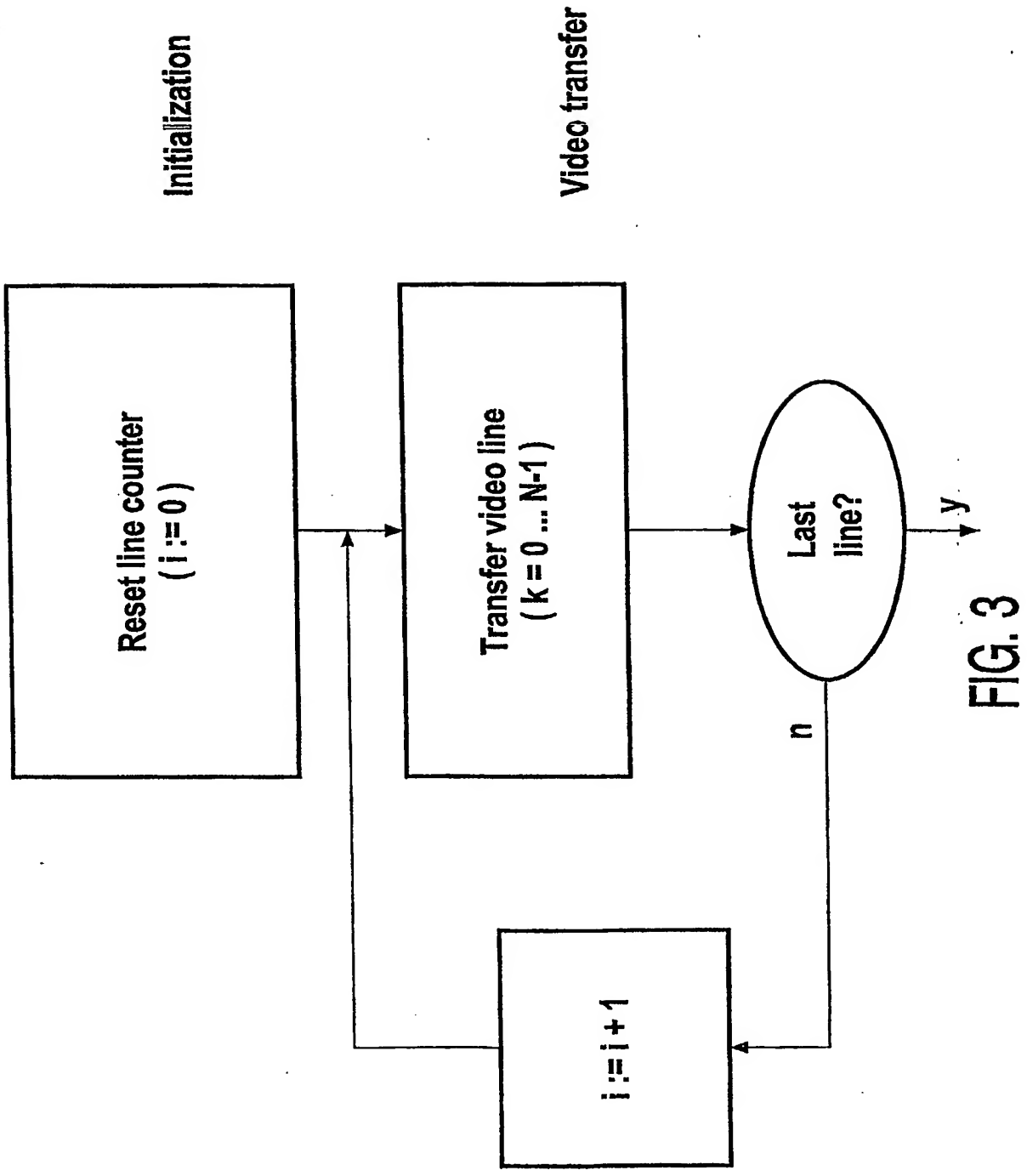
Initialization
Video transfer
Reset line counter
(i := 0)
Transfer video line
(k = 0 ... N-1)
Last
line?
y
n
i := i + 1

FIG. 3

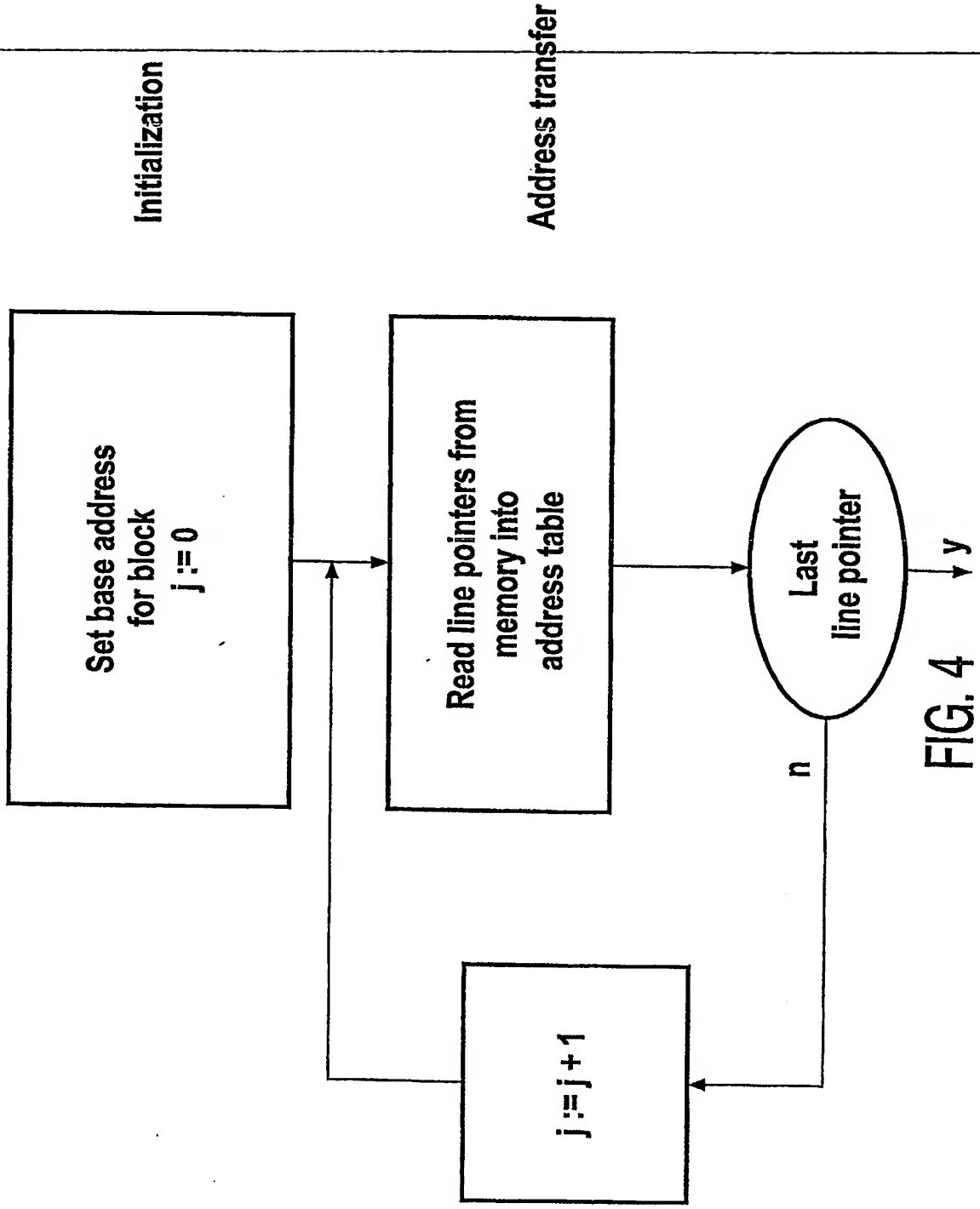
Initialization
Address transfer
Set base address for block j := 0
Read line pointers from memory into address table
Last line pointer
y
n
j := j + 1

FIG. 4

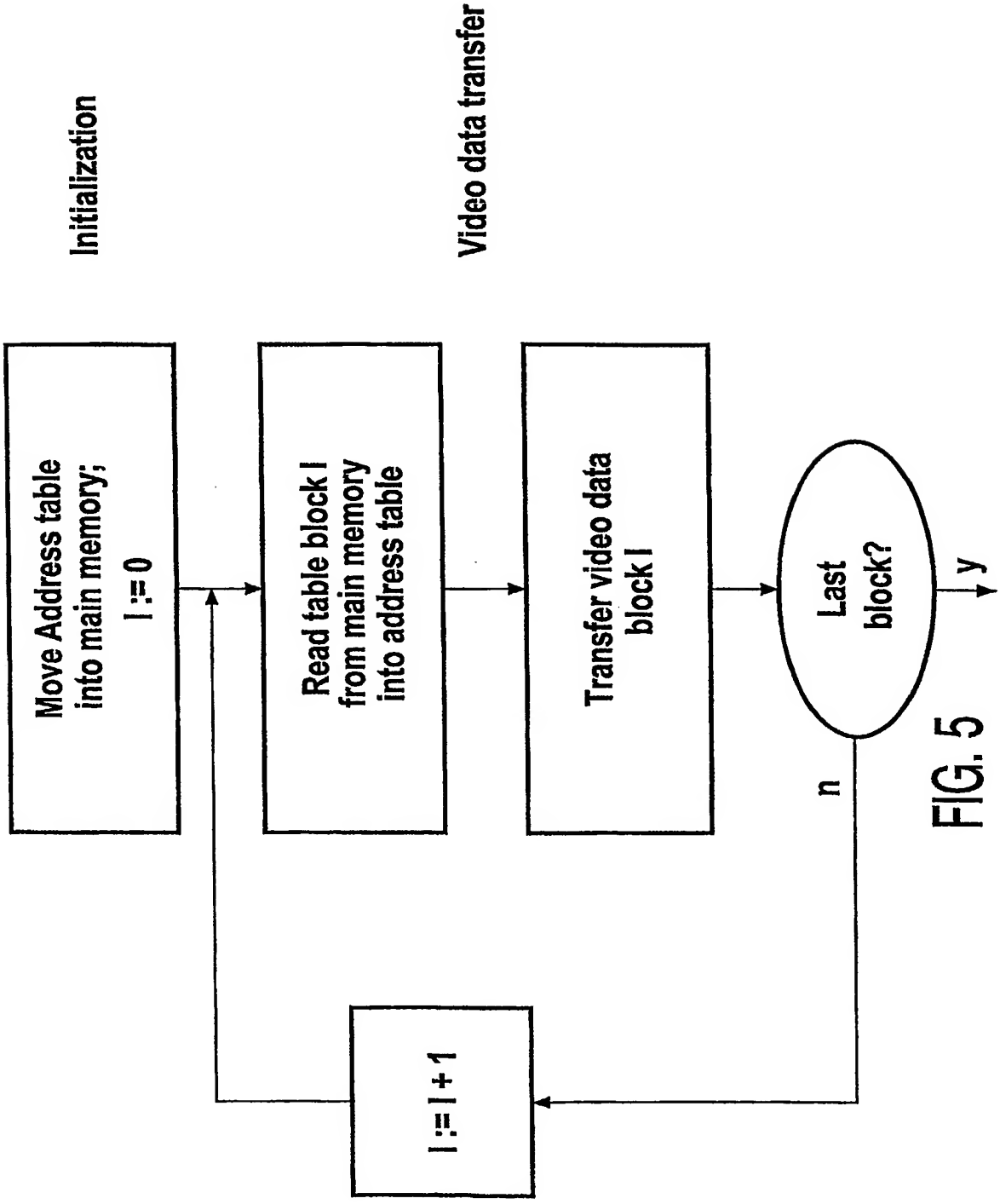
Initialization
Video data transfer
Move Address table into main memory; I := 0
Read table block I from main memory into address table
Transfer video data block I
Last block?
y
n
I := I + 1

FIG. 5

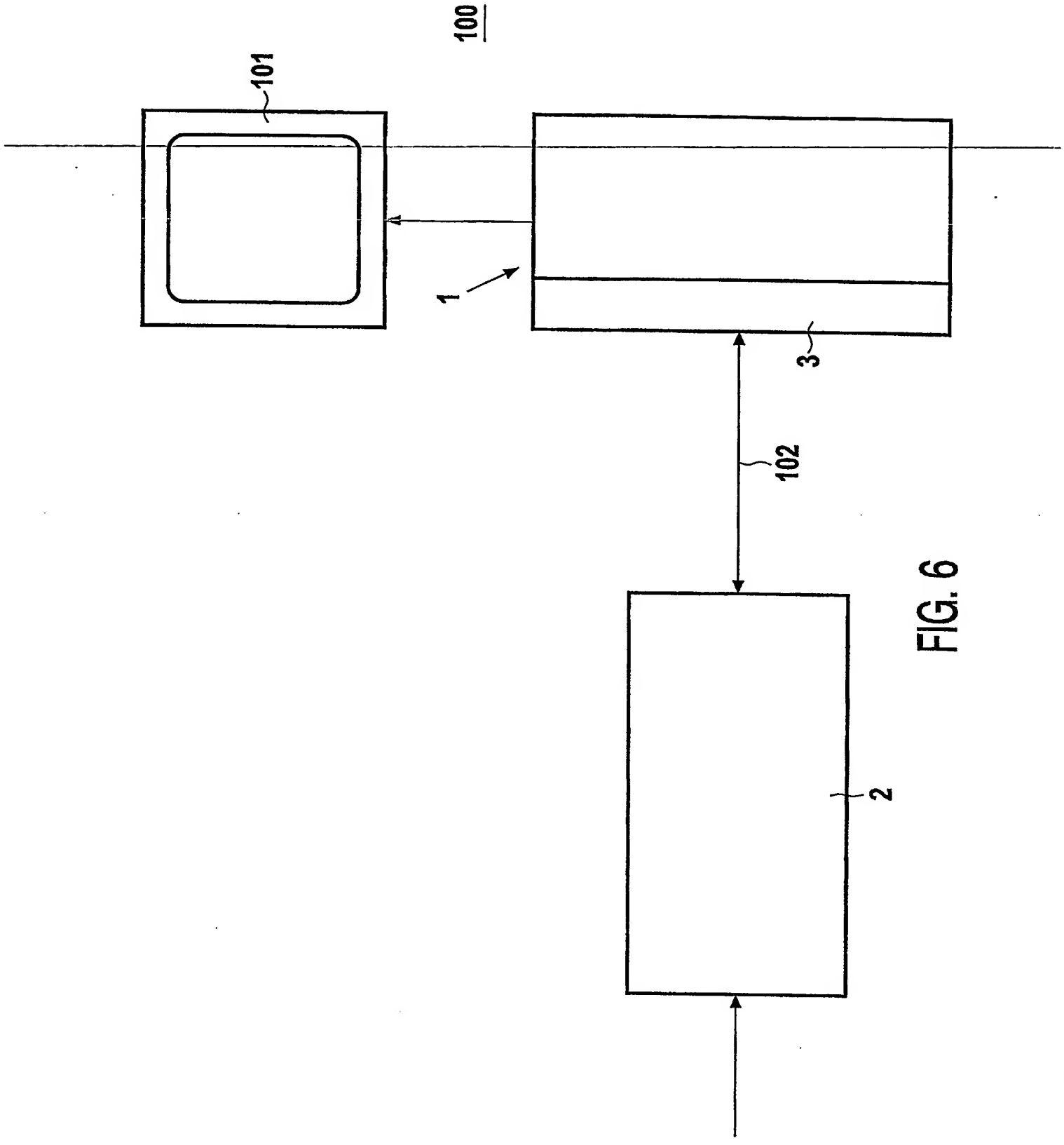

FIG. 6

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